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PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BY FACSIMILE TO EXAMINER M. Dimyan 703-872-9306
PLEASE HAND DELIVER TO EXAMINER Dimyan
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
TRANSMITTAL LETTER, FEE AUTHORIZATION
and RESPONSE TO OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In re: Patent Appln. USSN: 09/841,505 Filed: April 24, 2001 Action Day: Oct 29, 2004
Title: CMOS tapered gate and synthesis method
Inventor(s): Brian W. Curran et al.
Examiner: Magid Y Dimyan Group Art: 5674
Attorney Docket No.: PO9-2000-0107US1
Attorney/Agent: Lynn L. Augspurger, Reg. No.: 24,227 Deposit Acct: 09-0463

Dear Sir:

Please enter this 1.131 RESPONSE TO OFFICIAL ACTION, affidavits and remarks.

Please Amend the claims to read as follows:

1. (Currently Amended) A logic synthesis method for reducing the delay of a timing critical path in a circuit, comprising the steps of:

(a) selecting a gate which is not an inverter in the timing critical path [,];

(b) swapping said timing critical path to a pin of said gate [,];

(c) replacing said gate with a functionally equivalent tapered gate [,];

(d) performing a timing analysis of said circuit [,];